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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
WILLIAMS, ALEXANDER O	
ART UNIT	PAPER NUMBER
2826	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/16/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/680,664	KUO ET AL.	
	Examiner	**Art Unit**	
	Alexander O. Williams	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) d on *01 June 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3,5-11,13-15 and 17-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1, 3, 5-11, 13-15 and 17-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application

6) ☐ Other: _____.

Serial Number: 10/680664   Attorney's Docket #: 24061.43/TSMC2002-0978
Filing Date: 10/7/2003;

Applicant: Kuo et al.

Examiner: Alexander Williams

Applicant's Reason in Support of a Pre-Appeal Request for Review filed 6/1/06 to the election of species of figure 1 (claims 1 to 3 and 5 to 20), filed 4/12/05, has been acknowledged.

This application contains claim 4 drawn to an invention non-elected without traverse.

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 6/1/06 has been entered.

Claims 2, 12 and 16 have been cancelled.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 3, 5 to 11, 13 to 15 and 17 to 20 are rejected under 35 U.S.C. § 102(b) as being anticipated by Moslehi (U.S. Patent # 6,124,198).

1. Moslehi (figures 1 to 15) specifically figures 9, 10, 13 and 14 show an integrated circuit package bond pad **(electrode along M6)**, comprising: an insulating layer **(insulating layer along via plugs 5)**; an electrode located over the insulating layer and having a plurality of discrete conductors **(metal within the via above M6 shown in figure 13 and vias in figure 9)** separated by portions of dielectric layer **(dielectric within the layer above M6 shown in figure 13 and dielectric shown in figure 9)**, wherein each of the plurality of discrete conductors has a first surface configured to be bonded to external circuitry and a second surface opposite the first surface; and a plurality of conductive members **(conductor layers along M5)** located in the insulating layer, wherein ones of the plurality of conductive members contact the second surface of corresponding ones of the plurality of discrete conductors of the electrode.

(13) Subsequently, copper CMP and post-CMP clean processes are performed, at step 130, in order to form the embedded via copper plugs and inlaid interconnect metal lines. The repetitive steps of multi-layer dielectric stack deposition, fabrication of via holes and metal line trenches, copper deposition, and copper CMP (and post-CMP clean) are performed multiple times until all the necessary interconnect levels are fabricated, as verified at step 132. After formation of all the necessary interconnect levels, a top etch-resistant dielectric layer, preferably a silicon nitride layer (on the order of 2000 .ANG. to 1 .mu.m thick), is deposited by CVD, PECVD, or PVD, at step 134. Other suitable etch-resistant (and preferably high-thermal-conductivity dielectric materials) such as aluminum nitride or diamond-like carbon (DLC) may also be used instead of silicon nitride. The schematic diagram of FIG. 8 illustrates the example of a cross-sectional view of a multi-level interconnect structure (shown with six levels of copper interconnect) at this stage in the interconnect fabrication process flow.

(14) Next, a microlithography patterning process and a subsequent anisotropic RIE process are performed (see step 136) in order to form etchant transmission windows or openings within the top dielectric layer. The schematic diagrams on pages FIGS. 9, 10, 11 and 12 show several possible layout patterns of the etchant transmission windows, formed within the top etch-resistant dielectric layer. Preferably, the etchant transmission window pattern comprises openings or windows (squares, rectangular, circular, etc.) with at least one minimum-geometry in-plane dimension. For instance, the pattern of FIG. 9 shows an array of closely-spaced square windows. For a 0.18 .mu.m technology node, these windows may have 0.18 .mu.m.times.0.18 .mu.m areas and the adjacent windows may be separated by 0.18 .mu.m. The alternative pattern in FIG. 10 comprises an array of circular holes. Again, the holes may have minimum-geometry diameters (e.g., 0.18 .mu.m diametric dimensions for circular holes separated by 0.18 .mu.m from each other in a 0.18 .mu.m technology). FIGS. 10 and 11 show two alternative etchant transmission window patterns comprising rectangular windows with larger overall transmission window area ratios (ratio of total area of the windows to the total surface area). The smaller side dimensions of these rectangular windows are preferably the same as the resolution of the microlithography tool (e.g., 0.18 .mu.m for a 0.18 .mu.m technology), while the larger side dimensions (lengths of rectangular windows) may be several to tens to even hundreds of microns (.mu.m). The idea is to have an etchant transmission window pattern which provides a relatively large transmission area ratio (preferably .gtorsim.50%) and can be subsequently hermetically sealed using a simple deposition process without a significant impact on the interconnect metallization structure. Preferably, the thickness of the top etch-resistant layer (e.g. Si.sub.3 N.sub.4 or AIN layer deposited by CVD, PECVD, or PVD or any other vapor deposition process) is several times larger than the smaller side dimension of the etchant transmission unit cells. For instance, for a 0.18 .mu.m technology, we may use a 0.70 .mu.m-to-1 .mu.m thick silicon nitride top etch-resistant layer with etchant transmission window cells (square, circular, rectangular, or any other shape) which have 0.18 .mu.m minimum in-plane dimension (e.g., rectangular unit cells, with 0.18 .mu.m.times.5 .mu.m window size).

3. The bond pad of claim 1, Moslehi show wherein the plurality of conductive members each have a shape selected from the group consisting of: **a square cube**; a rectangular cube; and a cylinder.

5. The bond pad of claim 1, Moslehi show wherein at least two of the ones of the plurality of conductive members have a first size and at least two of the ones of the plurality of conductive members have a second size (both first and second sizes are the same).

6. The bond pad of claim 1, Moslehi show wherein the ones of the plurality of conductive members are first ones each having a first shape, wherein second ones of the plurality of conductive members each have a second shape.

7. The bond pad of claim 1, Moslehi show wherein each of the plurality of conductive members comprises a material selected from the group consisting of: **metal**; doped polysilicon; and metal silicide.

8. The bond pad of claim 1, Moslehi show wherein at least two of the plurality of conductive members are located in a portion of the insulating layer outside a perimeter of the electrode.

9. The bond pad of claim 1, Moslehi show wherein a volumetric ratio of the ones of the plurality of conductive members to the insulating layer ranges between about 1:1 and about 1:5. Note that the specification contains no disclosure of either the critical nature of the claimed dimensions or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. In re Woodruff, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

10. The bond pad of claim 1, Moslehi show wherein the first surface of the electrode has a serrated thickness profile.

11. Moslehi (figures 1 to 15) specifically figures 9, 10, 13 and 14 show a method of manufacturing an integrated circuit package bond pad **(electrode along M6)**, comprising: forming an insulating layer **(insulating layer along via plugs 5)** over a substrate **(silicon substrate**; forming a plurality of conductive members **(conductor layers along M5)** in the insulating layer; and forming an electrode **(electrode along M6)** over the insulating layer, the electrode having a plurality of discrete conductors **(metal within the via above M6 shown in figure 13 and vias in figure 9)** separated by portions of a dielectric layer **(dielectric within the layer above M6 shown in figure 13 and dielectric shown in figure 9)**, wherein each of the plurality of discrete conductors has: a first surface configured to be bonded to external circuitry; and a second surface opposite the first surface and contacting a corresponding one of the plurality of conductive members.

13. The method of claim 11, Moslehi show wherein forming the plurality of conductive members includes depositing a material selected from the group consisting of: **metal**; doped polysilicon; and metal silicide.

14. The method of claim 11, Moslehi show wherein the first surface of the electrode has a serrated thickness profile.

15. Moslehi (figures 1 to 15) specifically figures 9, 10, 13 and 14 show a method of manufacturing an electronic device, omprising: providing a substrate **(silicon substrate)** having a first bond pad **(electrode along M6)** located thereon; providing an integrated circuit package having a second bond pad **(electrode along M6)** located thereon, the second bond pad including: an insulating layer **(insulating layer along**

via plugs 5); an electrode **(electrode along M6)** located over the insulating layer and having a plurality of discrete conductors **(metal within the via above M6 shown in figure 13 and vias in figure 9)** separated by portions of a dielectric layer **(dielectric within the layer above M6 shown in figure 13 and dielectric shown in figure 9)**, wherein each of the plurality of discrete conductors has a first surface configured to be bonded to the first bond pad and a second surface opposite the first surface; and a plurality of conductive members **(conductor layers along M5)** located in the insulating layer, wherein ones of the plurality of conductive members contact the second surface of corresponding ones of the plurality of discrete conductors of the electrode; and forming a bond electrically coupling the first and second bond pads.

17. The method of claim 15, Moslehi show wherein the plurality of conductive members each have a rectangular cube shape.

18. The method of claim 15, Moslehi show wherein a volumetric ratio of the ones of the plurality of conductive members to the insulating layer ranges between about 1:1 and about 1:5. Note that the specification contains no disclosure of either the critical nature of the claimed dimensions or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. In re Woodruff, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

19. The method of claim 15, Moslehi show wherein the first surface of the electrode has a serrated thickness profile.

20. The method of claim 15, Moslehi show wherein forming a bond includes a process selected from the group consisting of: wire bonding; and surface mounting.

Claims 1, 3, 5 to 11, 13 to 15 and 17 to 20 are rejected under 35 U.S.C. § 102(e) as being anticipated by Seyyedy et al. (U.S. Patent # 7,126,200 B2).

1. Seyyedy et al. (figures 1 to 3) specifically figure 3 show an integrated circuit package bond pad **M3**, comprising: an insulating layer **(lower portion of 328)**; an electrode located over the insulating layer and having a plurality of discrete conductors **M4,343** separated by portions of dielectric layer **(upper portion of 328)**, wherein each of the plurality of discrete conductors has a first surface configured to be bonded to external circuitry and a second surface opposite the first surface; and a plurality of conductive members **M2,336** located in the insulating layer, wherein ones of the plurality of conductive members contact the second surface of corresponding ones of the plurality of discrete conductors of the electrode.

3. The bond pad of claim 1, Seyyedy et al. show wherein the plurality of conductive members each have a shape selected from the group consisting of: **a square cube**; a rectangular cube; and a cylinder.

5. The bond pad of claim 1, Seyyedy et al. show wherein at least two of the ones of the plurality of conductive members have a first size and at least two of the ones of the plurality of conductive members have a second size (both first and second sizes are the same).

6. The bond pad of claim 1, Seyyedy et al. show wherein the ones of the plurality of conductive members are first ones each having a first shape **(134,square cube)**, wherein second ones of the plurality of conductive members each have a second shape **(134,square cube)**.

7. The bond pad of claim 1, Seyyedy et al. show wherein each of the plurality of conductive members comprises a material selected from the group consisting of: **metal**; doped polysilicon; and metal silicide.

8. The bond pad of claim 1, Seyyedy et al. show wherein at least two of the plurality of conductive members are located in a portion of the insulating layer outside a perimeter of the electrode.

9. The bond pad of claim 1, Seyyedy et al. show wherein a volumetric ratio of the ones of the plurality of conductive members to the insulating layer ranges between about 1:1 and about 1:5. Note that the specification contains no disclosure of either the critical nature of the claimed dimensions or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. In re Woodruff, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

10. The bond pad of claim 1, Seyyedy et al. show wherein the first surface of the electrode has a serrated thickness profile.

11. Seyyedy et al. (figures 1 to 3) specifically figure 3 show a method of manufacturing an integrated circuit package bond pad **M3**, comprising: forming an insulating layer **(328 under M3)** over a substrate **308**; forming a plurality of conductive members **M2,336** in the insulating layer; and forming an electrode **M3** over the insulating layer, the electrode having a plurality of discrete conductors **M4,343** separated by portions of a dielectric layer **(328 under portion above M3)**, wherein each of the plurality of discrete conductors has: a first surface configured to be bonded to external circuitry; and a second surface opposite the first surface and contacting a corresponding one of the plurality of conductive members.

13. The method of claim 11, Seyyedy et al. show wherein forming the plurality of conductive members includes depositing a material selected from the group consisting of: **metal**; doped polysilicon; and metal silicide.

14. The method of claim 11, Seyyedy et al. show wherein the first surface of the electrode has a serrated thickness profile.

15. Seyyedy et al. (figures 1 to 3) specifically figure 3 show a method of manufacturing an electronic device, comprising: providing a substrate **308** having a first bond pad **M3,342** located thereon; providing an integrated circuit package having a second bond pad **M3,342** located thereon, the second bond pad including: an insulating layer **(portion of M3,342 under M3)**; an electrode **M3,342** located over the insulating layer and having a plurality of discrete conductors **M4,343** separated by portions of a dielectric layer **(portion of 328 above M3)**, wherein each of the plurality of discrete conductors has a first surface configured to be bonded to the first bond pad and a second surface opposite the first surface; and a plurality of conductive members **M2,336** located in the insulating layer, wherein ones of the plurality of conductive members contact the second surface of corresponding ones of the plurality of discrete conductors of the electrode; and forming a bond electrically coupling the first and second bond pads.

17. The method of claim 15, Seyyedy et al. show wherein the plurality of conductive members each have a rectangular cube shape.

18. The method of claim 15, Seyyedy et al. show wherein a volumetric ratio of the ones of the plurality of conductive members to the insulating layer ranges

between about 1:1 and about 1:5. Note that the specification contains no disclosure of either the critical nature of the claimed dimensions or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. In re Woodruff, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

19. The method of claim 15, Seyyedy et al. show wherein the first surface of the electrode has a serrated thickness profile.

20. The method of claim 15, Seyyedy et al. show wherein forming a bond includes a process selected from the group consisting of: wire bonding; and surface mounting.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Initially, it is noted that the 35 U.S.C. § 103 rejection based on an electrode and a plurality of electrodes deals with an issue (i.e., the integration of multiple pieces into one piece or conversely, using multiple pieces in replacing a single piece) that has been previously decided by the courts.

In Howard v. Detroit Stove Works 150 U.S. 164 (1893), the Court held, "it involves no invention to cast in one piece an article which has formerly been cast in two pieces and put together...."

In In re Larson 144 USPQ 347 (CCPA 1965), the term "integral" did not define over a multi-piece structure secured as a single unit. More importantly, the court went further and stated, "we are inclined to agree with the solicitor that the use of a one-piece construction instead of the [multi-piece] structure disclosed in Tuttle et al. would be merely a matter of obvious engineering choice" (bracketed material added). The court cited In re Fridolph for support.

In re Fridolph 135 USPQ 319 (CCPA 1962) deals with submitted affidavits relating to this issue. The underlying issue in In re Fridolph was related to the end result of making a multi-piece structure into a one-piece structure. Generally, favorable patentable weight was accorded if the one-piece structure yielded results not expected from the modification of the two-piece structure into a single piece structure.

Claims 1, 3, 5 to 11, 13 to 15 and 17 to 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yu et al. (U.S. Patent # 6,703,286 B1).

1. Yu et al. (figures 1 to 6) specifically figure 6 show an integrated circuit package bond pad **14**, comprising: an insulating layer **52**; an electrode **(the plurality of 14's)** located over the insulating layer and having a plurality of discrete conductors **60** separated by portions of dielectric layer **58**, wherein

each of the plurality of discrete conductors has a first surface configured to be bonded to external circuitry and a second surface opposite the first surface; and a plurality of conductive members **54** located in the insulating layer **52,** wherein ones of the plurality of conductive members contact the second surface of corresponding ones of the plurality of discrete conductors **60** of the electrode.

(30) In accordance with the objectives of the invention a new method is provided for the fabrication of bond pads on a semiconductor die. The shape of the Prior Art bond pad is altered where one (large) pad is divided into many (smaller) pads, the (smaller) pads that belong to the same interconnect level and that are part of one metal bond pad are interconnected. A dielectric is deposited over the pattern of (smaller) pads, openings are made in the dielectric that match the patterns of smaller pads. A square opening is created overlying the created smaller pads and filled with metal joining the newly created square metal bond pad with the preceding patterns of small metal pads.

3. The bond pad of claim 1, Yu et al. show wherein the plurality of conductive members each have a shape selected from the group consisting of: **a square cube**; a rectangular cube; and a cylinder.

5. The bond pad of claim 1, Yu et al. show wherein at least two of the ones of the plurality of conductive members **(54, first two on the right)** have a first size and at least two of the ones of the plurality of conductive members **(54, first two on the left)** have a second size (both first and second sizes are the same).

6. The bond pad of claim 1, Yu et al. show wherein the ones of the plurality of conductive members are first ones each having a first shape **(54,square cube)**, wherein second ones of the plurality of conductive members each have a second shape **(54,square cube)**.

7. The bond pad of claim 1, Yu et al. show wherein each of the plurality of conductive members comprises a material selected from the group consisting of: **metal**; doped polysilicon; and metal silicide.

8. The bond pad of claim 1, Yu et al. show wherein at least two of the plurality of conductive members **(54)** are located in a portion of the insulating layer **52** outside a perimeter of the electrode.

9. The bond pad of claim 1, Yu et al. show wherein a volumetric ratio of the ones of the plurality of conductive members **54** to the insulating layer **302** ranges between about 1:1 and about 1:5. Note that the specification contains no disclosure of either the critical nature of the claimed dimensions or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. In re Woodruff, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

10. The bond pad of claim 1, Yu et al. show wherein the first surface of the electrode has a serrated thickness profile.

11. Yu et al. (figures 1 to 6) specifically figure 6 show a method of manufacturing an integrated circuit package bond pad **14** comprising: forming an insulating layer **52** over a substrate **70**; forming a plurality of conductive members **54** in the insulating layer; and forming an electrode **(plurality of 14's)** over the insulating layer, the electrode having a plurality of discrete conductors **60** separated by portions of a dielectric layer **58**, wherein each of the plurality of discrete conductors has: a first surface configured to be bonded to external circuitry; and a second surface opposite the first surface and contacting a corresponding one of the plurality of conductive members.

13. The method of claim 11, Yu et al. show wherein forming the plurality of conductive members includes depositing a material selected from the group consisting of: **metal**; doped polysilicon; and metal silicide.

14. The method of claim 11, Yu et al. show wherein the first surface of the electrode has a serrated thickness profile.

15. Yu et al. (figures 1 to 6) specifically figure 6 show a method of manufacturing an electronic device, comprising: providing a substrate **70** having a first bond pad **(** located thereon; providing an integrated circuit package having a second bond pad **133,134,204** located thereon, the second bond pad including: an insulating layer **130**; an electrode **134** located over the insulating layer and having a plurality of discrete conductors **204** separated by portions of a dielectric layer **138**, wherein each of the plurality of discrete conductors has a first surface configured to be bonded to the first bond pad and a second surface opposite the first surface; and a plurality of conductive members **133,134** located in the insulating layer, wherein ones of the plurality of conductive members contact the second surface of corresponding ones of the plurality of discrete conductors of the electrode; and forming a bond electrically coupling the first and second bond pads.

17. The method of claim 15, Yu et al. show wherein the plurality of conductive members **54** each have a rectangular cube shape.

18. The method of claim 15, Yu et al. show wherein a volumetric ratio of the ones of the plurality of conductive members to the insulating layer ranges between about 1:1 and about 1:5. Note that the specification

contains no disclosure of either the critical nature of the claimed dimensions or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. In re Woodruff, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

19. The method of claim 15, Yu et al. show wherein the first surface of the electrode has a serrated thickness profile.

20. The method of claim 15, Yu et al. show wherein forming a bond includes a process selected from the group consisting of: wire bonding; and surface mounting.

Therefore, it would have been obvious to one of ordinary skill in the art to use the **electrode and the plurality of electrodes** as "merely a matter of obvious engineering choice" as set forth in the above case law.

Response

Applicant's arguments filed 6/1/06 have been fully considered, but are moot in view of the new grounds of rejections detailed above.

The listed references are cited as of interest to this application, but not applied at this time.

Field of Search	Date
U.S. Class and subclass: 257/758,701,700,698,696,781,784,786,774,734,773,779, 780,750,751,173,e23.03,e21.508,e23.144,e23,167 438/613,617,612,624,626,639,637	6/24/05 12/8/05 1/2/07
Other Documentation: foreign patents and literature in 257/758,701,700,698,696,781,784,786,774,734,773,779, 780,750,751,173,e23.03,e21.508, e23.144,e23,167 438/613,617,612,624,626,639,637	6/24/05 12/8/05 1/2/07
Electronic data base(s): U.S. Patents EAST	6/24/05 12/8/05

	1/2/07

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexander O. Williams whose telephone number is (571) 272 1924. The examiner can normally be reached on M-F 6:30-7:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272 1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Alexander O Williams
Primary Examiner
Art Unit 2826

AOW
1/2/07